AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A platform comprising:

a processor to execute ~~executing~~ in one of a normal execution mode and an isolated execution mode, the processor to issue isolated access bus cycles, the isolated access bus cycles identifiable by a processor interface signal indicating an isolated attribute;

a system memory accessible to the processor and including an isolated area, an isolated output area to store output data, and a non-isolated area, the processor permitted to write the output data into the isolated output area only when the processor issues the isolated access bus cycles; and

a graphics card coupled to the processor, ~~and accessible to different areas of the system memory according to access modes asserted by the graphics card~~the graphics card permitted to read the output data from the isolated output area only in the isolated execution mode.

2. (Currently Amended) The platform of claim 1 wherein the graphics card comprises logics to handle the output data from the isolated output area and the non-isolated area differently.

3. (Previously Presented) The platform of claim 2 further comprising:

a memory control hub (MCH) coupled between the system memory, the processor, and the graphics card, the memory control hub to permit the graphics card to access the isolated output area only when the graphics card asserts an isolated access mode.

4. (Currently Amended) The platform of claim 3 wherein the graphics card comprises:

a direct memory access (DMA) controller ~~and wherein local storage of the data in the graphics card from the isolated output area is not permitted~~to request bit map in the isolated output area be directly sent to an output end point.

5. (Original) The platform of claim 3 wherein only the graphics card is permitted to read the isolated output area.

6. (Previously Presented) The platform of claim 1 further comprising:

an operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in the isolated execution mode.

7. (Original) The platform of claim 3 further comprising:

a link between the graphics card and the MCH having an isolated transaction type.

8. (Original) The platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area.

9. (Original) The platform of claim 7 wherein the link is a secure accelerated graphics port bus.

10. (Previously Presented) The platform of claim 2 wherein the graphics card comprises:

an isolated bit plane for the output data from the isolated output area; and

a non-isolated bit plane for the output data from the non-isolated output area.

11. (Original) The platform of claim 10 wherein the graphics card denies all external access to the isolated bit plane.

12. (Currently Amended) A method comprising:

establishing an isolated execution environment having an isolated execution mode by a processor issuing isolated access bus cycles, the isolated access bus cycles identifiable by a processor interface signal indicating an isolated attribute~~providing hardware support for the isolated execution mode~~; and

preventing access to output data in an isolated output area of a system memory by any requester not operating in the isolated execution mode, the access including the processor writing the output data into the isolated output area and a graphics card reading the output data from the isolated output area~~; and~~

~~handling the output data from the isolated output area and non-isolated area of the system memory differently at a graphics card that operates, and has different memory access privileges, in a normal execution mode and the isolated execution mode~~.

13. (Canceled)

14. (Previously Presented) The method of claim 12 further comprising:

issuing an isolated direct memory access (DMA) request for display data in the isolated output area from the graphics card; and

refreshing the display based on the display data.

15. (Previously Presented) The method of claim 12 wherein preventing comprises:

identifying if an isolated attribute is present in a request for access to the isolated output area; and

denying the request if no isolated attribute is present.

16. (Previously Presented) The method of claim 12 further comprising:

loading data from the isolated output area into a bit plane on the graphics card; and

denying all external access to the bit plane.

17. (Previously Presented) The method of claim 16 further comprising:

defining a first window on an output display to present an image corresponding to the bit plane; and

occluding all windows on the display but the first window.

18. (Previously Presented) The method of claim 12 further comprising:

retrieving data from the isolated output area;

displaying an image corresponding to the data; and

occluding the image prior to a platform transitioning out of the isolated execution mode.

19. (Currently Amended) A platform comprising:

a processor executing in one of a normal execution mode and an isolated execution mode, the processor to issue isolated access bus cycles, the isolated access bus cycles identifiable by a processor interface signal indicating an isolated attribute to a memory controller hub (MCH);

a direct memory access (DMA) controller to issue requests for access to an isolated output area of a system memory ~~that includes the isolated output area and a non-isolated area~~, the isolated output area writable by the processor only when the processor issues the isolated access bus cycles;

a first interface coupled to the DMA controller to forward requests to ~~a~~ the MCH~~memory control hub (MCH)~~; and

a graphics card coupled to the MCH to supply output data to an output device, the graphics card permitted to read the output data from the isolated output area only in the isolated execution mode~~accessible to different areas of the system memory according to access modes asserted by the graphics card~~.

20. (Original) The apparatus of claim 19 wherein the first interface is a secure accelerated graphics port (AGP) and the output device is a display.

21. (Original) The apparatus of claim 19 wherein the DMA controller attaches an isolated attribute to any isolated output area access request.

22. (Previously Presented) The apparatus of claim 19 wherein the graphic card comprises logics to handle the output data from the isolated output area and the non-isolated area differently.